Please amend the paragraph beginning on page 1, line 9 (added by a Preliminary Amendment filed 31 August 1999) to read as follows:

> This is a continuation application of International PCT Patent Application No. PCT/US99/02504, designating the US, filed February 4, 1999, entitled METHOD AND APPARATUS FOR LOW TEMPERATURE ANNEALING OF METALLIZATION MICRO-STRUCTURES IN THE PRODUCTION OF A MICROELECTRONIC DEVICE, which claims priority from US Patent Application Serial No. 09/018,783, filed February 4, 1998, and US Patent Application Serial No. 60/087,432 filed June 1, 1998.

Please amend the paragraph extending from page 14, line 17 to page 15, line 2 to read as follows:

> The semiconductor wafer with the seed layer 425 is subject to a subsequent electrochemical copper deposition process. The electrochemical copper deposition process is executed so as to form numerous nucleation sites for the copper deposition to thereby form grain sizes that are substantially smaller than the characteristic dimensions of the via 420 and trench 415. An exemplary structure having such characteristics is illustrated in Fig. 2E wherein layer 440 is a layer of copper metallization that has been deposited using an electrochemical deposition process.

Please amend the paragraph extending from page 15, line 16, to page 16, line 9 as follows:

> A comparison between Figs. 2E and 2F reveals that an increase in the grain size of the copper layer 440 has taken place. Traditionally, the change in the grain size has been forced through an annealing process. In such an annealing process, the wafer is subject to an elevated temperature that is substantially above the ambient temperature conditions normally found in a clean room. For example, such annealing usually takes place in a furnace having a temperature generally around or slightly below 400 degrees Celsius, or about half

of the melting temperature of the electrodeposited copper. Annealing steps are normally performed at a temperature of at least 25 percent of the melting point temperature of the material as measured on an absolute temperature scale. As such, a separate annealing step is performed on the wafer using a separate piece of capital equipment. Such an annealing step is usually performed for each layer of metallization that is deposited on the wafer. These additional steps increase the cost of manufacturing devices from the wafer and, further, provide yet another step in which the wafer may be mishandled, contaminated or otherwise damaged.

Please amend the paragraph extending from page 17, line 10, to page 18, line 2 to read as follows:

The electrochemical plating solution may be Enthone-OMI Cu Bath M Make-up Solution having 67 g/l of $CuSO_4$, 170 g/l of H_2SO_4, and 70 ppm of HCl. The additive solutions utilized may be Enthone-OMI Cu Bath M-D (6.4 ml/l - make-up) and Enthone-OMI Cu Bath M LO 70/30 Special (1.6 ml/l - make-up). The flow rate through the cup 25 of this solution may be approximately 1.0 - 10 GPM (preferably 5.5 GPM) and the plating temperature may be between about 10-40 degrees Celsius (preferably 25 degrees Celsius). The plating bath could alternatively contain any of a number of additives from manufacturers such as Shipley (Electroposit 1100), Lea Ronal (Copper Gleam PPR), or polyethylene glycol (PEG). An alkaline plating bath suitable for electroplating microelectronic components is set forth in co-pending provisional patent application U.S.S.N. 60/085,675, filed 15 May 1998 and entitled "PROCESS AND PLATING SOLUTION FOR ELECTROPLATING A COPPER METALLIZATION LAYER ONTO A WORKPIECE" which is hereby incorporated by reference.

IN THE CLAIMS: